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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,951	11/14/2003	Abiola Awujoola	03-1025	6949

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EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,951	AWUJOOLA ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-19, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le Coz (US Patent Application Publication 2001/0039644) in view of Polsky (US Patent Application Publication 2005/0104187).

As for the claims, Le Coz discloses the invention substantially as claimed, including:

1. An apparatus for packaging and providing backside access to an integrated circuit, the apparatus comprising:
a carrier substrate [fig. 2A, paragraphs 0003, 0008, 0010-0011, 0028, and 0082];
an array of package connection pads positioned around a periphery of a top surface of the carrier substrate [fig. 2a, pg. 3, table 1, die-up, paragraphs –57-0058, 0078, and 0081-0082];
a ring of die connection pads positioned within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die [fig. 2a, pg. 3, table 1, die-up, paragraphs –57-0058, 0078, and 0081-0082];
2. The apparatus of claim 1, wherein the carrier substrate comprises a plurality of

circuit traces configured to electrically connect the array of package connection pads to the ring of die connection pads without penetrating the access region [fig. 2A, paragraphs 0077,-0078, 0081-0082];

3. The apparatus of claim 1, wherein the array of package connection pads has a perimeter depth substantially equal to a maximum number of signal traces routable between minimally spaced package connection pads [fig. 2A, paragraphs 0077,-0078, 0081-0082 – the perimeter depth and spacing are user definable];

4. The apparatus of claim 1, wherein the array of package connection pads has a perimeter depth that is less than a package connection pad spacing divided by a trace pitch [fig. 2A, paragraphs 0077,-0078, 0081-0082 – the perimeter depth, spacing and pitch are user definable];

5. The apparatus of claim 1, wherein the carrier substrate comprises a single signal layer [fig. 2A, paragraphs 0013, 0077,-0078, 0081-0082 – the layers are user definable];

6. The apparatus of claim 1, wherein the access region corresponds to a substrate cavity [fig. 2A, paragraphs 0013, 0077,-0078, 0081-0082 – the access region (cavity) is user definable];

7. The apparatus of claim 6, wherein the integrated circuit die is positioned within the substrate cavity [fig. 2A, paragraphs 0013, 0077,-0078, 0081-0082 – the positioning of the die is user definable];

8. The apparatus of claim 7, further comprising a package body molded over the integrated circuit die [fig. 2A, paragraphs 0013, 0077,-0078, 0081-0082 – the package body user definable, for example, die-up or die-down];

9. The apparatus of claim 1, further comprising a heat spreader thermally connected to a bottom surface of the substrate [Fig. 2C – Thermal balls];

10. The apparatus of claim 1, wherein the ring of die connection pads comprises a quadrant of bonding fingers that are substantially equally distanced from an edge of the integrated circuit die [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021 – the ring of die connection pads including a quadrant of bonding fingers equally distanced are user definable];

11. The apparatus of claim 1, further comprising at least one grounding ring surrounding

the access region [paragraph 0082];

12. The apparatus of claim 1, further comprising an array of solder balls attached to the array of package connection pads [paragraph 0028];.

13. The apparatus of claim 1, wherein the carrier substrate is a printed circuit board [paragraphs 0010-0013 and 0033 – the substrate may be various chip carriers including a printed circuit board];

14. The apparatus of claim 1, wherein the array of package connection pads is configured to receive an array of solder balls [paragraph 0028];

15. A method for designing an integrated circuit carrier to an integrated circuit, the method comprising:

placing an array of package connection pads around a periphery of a top surface of a carrier substrate [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021 die-up];

placing a ring of die connection pads within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

16. The method of claim 15, further comprising placing at least one grounding ring surrounding the access region [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

17. The method of claim 15, further comprising selecting a perimeter depth for the array of package connection pads that is less than an package connection pad spacing divided by a trace pitch [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021 – especially paragraph 0082, the perimeter depth is user definable];

18. The method of claim 15, further comprising selecting a quadrant shape for a quadrant of bonding fingers such that the bonding fingers are substantially equally distanced to an edge of an integrated circuit die [fig. 2A, paragraphs 0013, 0028-0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021, the quadrant and spacing of fingers is user definable];

19. The method of claim 15, further comprising routing a plurality of traces between a

ring of die connection pads and an array of package connection pads without penetrating the access region [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

24. A system for packaging and providing backside access to a wide variety of integrated circuits, the system comprising:

a plurality circuit carriers, each circuit carrier configured to receive a range of integrated circuit sizes and I/0 counts, each circuit carrier overlapping in size range with at least one other circuit carrier of the plurality of circuit carriers, each circuit carrier comprising:

a carrier substrate [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

an array of package connection pads positioned around a periphery of a top surface of the carrier substrate [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

a line of die connection pads positioned within the array of package connection pads [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

25. The system of claim 24, wherein each circuit carrier overlaps in size range with no more than two other circuit carriers of the plurality of circuit carriers [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021 – the sizes are user definable];

Le Coz does not specifically disclose an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die without damaging electrical integrity of the carrier substrate; reserving an access region for conducting backside access to the integrated circuit; and an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die without damaging electrical integrity of the carrier substrate.

Polsky discloses an access region positioned within the ring for backside access without damaging the electrical integrity of the carrier substrate [abstract; paragraphs 0003, 0005 0031-0033, 0037-38].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Le Coz and Polsky because using Polsky's backside interconnects within a desired region of Le Coz's system would have provided Le Coz system of die-up or cavity type die to be accessed without damaging the carrier substrate through Polsky's predetermined interconnect locations without having to remove substrate material to minimize damages to the substrate carrier.

2. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le Coz (US Patent Application Publication 2001/0039644) in view of Li (US Patent 6,677,169).

As for the claims, Le Coz discloses the invention substantially as claimed, including:

20. A method for packaging and providing access to an integrated circuit, the method comprising:
electrically connecting an integrated circuit die to a ring of die connection pads on a top surface of a carrier substrate [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];
attaching a cover to a bottom surface of the carrier substrate [pg. 1, shows various configurations for the carrier that would inherently include a covering to a bottom surface of the carrier substrate];
21. The method of claim 20, further comprising placing the integrated circuit die within a cavity of the carrier substrate [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];
22. The method of claim 20, further comprising molding a package body over the

integrated circuit die [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];
23. The method of claim 20, further comprising attaching an array of solder balls to the array of package connection pads [fig. 2A, paragraphs 0013, 0029, 0077,-0078, 0081-0082, 0093-0094, Table 0021];

Le Coz does not specifically disclose removing a portion of the cover within an access region in order to access a backside of the integrated circuit without damaging electrical connectivity of the substrate.

Li discloses removing a portion of the cover within an access region in order to access a backside of the integrated circuit without damaging electrical connectivity of the substrate [abstract, col. 2, line 28 – col. 3, line 5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Le Coz and Li because utilizing Li's removal of a portion of the cover in order to access the backside of the IC without damaging electrical connectivity of the substate would have allowed for Le Coz system to gain access for backside analysis without damaging electrical connectivity which is required for certain circuit fault analysis [see Li, col. 2, especially lines 37-45].

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW